to the control gate, the potential difference between first well region and the control gate can be enlarged relatively while the maximum voltage in the semiconductor substrate can be lowered, and thus channel FN can be generated which enables writing/erasing operations. As described above, in the nonvolatile semiconductor memory device, since maximum voltage in the semiconductor device can be lowered, load to the peripheral circuitry can be reduced and therefore it is advantageous for higher degree of integration.

In addition, in the nonvolatile semiconductor memory device in accordance with the present invention, subbit lines are connected to respective drain regions of a plurality of memory transistors. Therefore, at the time of reading, a large read current can be obtained, which enables higher reading operation as compared with a NAND type device.

Further, in the nonvolatile semiconductor memory device in accordance with the present invention, the bit line is divided into a main bit line and a subbit line. The main bit line and the subbit line are made conductive through a select gate transistor. Therefore, one subbit line can be electrically separated from the other subbit line, while they share the main bit line. Accordingly, when writing operation is being carried out by using one subbit line, the other subbit line can be electrically separated from said one subbit line, and therefore in this writing operation, drain disturb is not caused in the memory transistors connected to the said the other bit line. Thus, by the nonvolatile semiconductor memory device, drain disturb can be reduced.

Further, in the nonvolatile semiconductor memory device in accordance with the present invention, data writing operation can be carried out by drain FN. Therefore, writing operation can be carried out with high efficiency with smaller current flowing through the bit lines. Since the current flowing through the bit line can be reduced, a material having larger resistance value can be used as the bit line, and therefore bit lines can be formed by using materials other than aluminum. Therefore two-layered structure of the main bit line and the subbit line and miniaturization of the bit lines can be simultaneously enabled.

In the nonvolatile semiconductor memory device in accordance with the present invention, memory transistors can be set to the written state by drain FN. Therefore, compared with the NOR type device in which writing operation is carried out by using channel hot electrons, efficiency in writing can be improved, and thus power consumption can be reduced.

By the nonvolatile semiconductor memory device in accordance with the present invention, the operation in accordance with the present invention can be carried out more stably.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a main bit line formed of metal wiring on said substrate;

first and second subbit lines connected in series, each formed of metal wiring and aligned parallel to said main bit line on said substrate;

first and second switching transistors, each responsive to a sector select signal for connecting said main bit line to a corresponding one of said first and second subbit lines,

a first memory cell group including a plurality of memory cells, each connected to said first subbit line; and

a second memory cell group including a plurality of memory cells, each connected to said second subbit line;

wherein

each of said memory cells includes a control gate and a floating gate formed on said substrate, and a source and a drain formed in a substrate area, and

each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain; said device further comprising

an insulating layer formed in a substrate area for insulating a memory cell in said first memory cell group located closest to said second memory cell group from a memory cell in said second memory cell group located closest to said first memory cell group.

2. A nonvolatile semiconductor memory device comprising:

a main bit line formed of metal wiring;

first and second subbit lines connected in series, each formed of metal wiring and aligned parallel to said main bit line;

first and second switching transistors, each responsive to a sector select signal for connecting said main bit line to a corresponding one of said first and second subbit lines;

a first memory cell group including n memory cells ($n \geq 2$), each connected to said first subbit line;

a second memory cell group including n memory cells, each connected to said second subbit line;

wherein

each of said memory cells includes a control gate, a floating gate, a drain, and a source, and

each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain; said device further comprising

n connection lines, each for connecting the control gate of a j-th memory cell ($j=1, 2, \ldots, n$) in said first memory cell group located in a direction farther from said second memory cell group to the control gate of a j-th memory cell in said second memory cell group located in a direction farther from said first memory cell group; and

row decoder means responsive to an externally applied address signal for selecting one of said n connection lines.

* * * * *

3. A nonvolatile semiconductor memory device, comprising:

a main bit line;

first and second subbit lines connected in series, each aligned parallel to said main bit line;

first and second switching transistors, each for connecting said main bit line to a corresponding one of said first and second subbit lines;

a first memory cell group including n ($n \geq 2$) memory cells, each connected to said first subbit line,

wherein

each of said memory cells includes a control gate, a floating gate, a drain and a source, and

each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain,

said device further comprising:

n connection lines, each for connecting the control gate of a relevant memory cell in said first memory cell group to the control gate of a corresponding memory cell in said second memory cell group; and

a row decoder, responsive to an externally applied address signal for selecting one of said n connection lines.

4. The nonvolatile semiconductor memory device according to claim 3, wherein said n connection lines are formed of polycrystalline silicon, and wiring for connection between said row decoder and said n connecting lines is formed of metal wiring.

5. A nonvolatile semiconductor memory device, comprising:

a first bit line including a metal film;

a switch having an end connected to said fist bit line;

a second bit line including polycrystalline silicon and connected to other end of said switch; and

a plurality of memory cells connected to said second bit line, each including a drain, a control gate, a floating gate and a source.

6. The nonvolatile semiconductor memory device according to claim 5, wherein said first bit line is placed in an upper layer of said second bit line.

7. A nonvolatile semiconductor memory device, comprising:

a first bit line;

a switch having a conductive end connected to said first bit line;

a second bit line connected to other conductive end of said switch;

a plurality of memory cells connected to said second bit line, each including a drain, a control gate, a floating gate and a source; and

a source line formed with an active layer, to which said sources of said memory cells are commonly connected.

8. The nonvolatile semiconductor memory device according to claim 7, wherein said first bit line is wiring including a metal film.

9. The nonvolatile semiconductor memory device according to claim 7, wherein said second bit line is wiring including polycrystalline silicon.

10. A nonvolatile semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of word lines provided corresponding to said rows;

a plurality of bit lines provided corresponding to said columns; and

a source line provided commonly for said plurality of memory cells,

wherein

each of said memory cells includes a control gate connected to corresponding said word line, a drain connected to corresponding said bit line, a source connected to said source, and a floating gate, and

electrons are extracted from the floating gate of each said memory cell via the drain of said memory cell.

11. The nonvolatile semiconductor memory device according to claim 10, further comprising an electron extracting means for extracting the electrons from the floating gate of selected said memory cell,

said electron extracting means including

means for applying a prescribed positive voltage to the selected bit line, and

means for applying a prescribed voltage to the selected word line.